LM3430 Boost Controller for LED Backlighting

Check for Samples: LM3430

FEATURES

- **Internal 40V Startup Regulator**
- **1A Peak MOSFET Gate Driver**
- **V_{IN} Range 6V to 40V**
- **Duty Cycle Limit in Excess of 90%**
- **Programmable UVLO with Hysteresis**
- **Cycle-by-Cycle Current Limit**
- **External Synchronizable (AC-coupled)**
- **Single Resistor Oscillator Frequency Set**
- **Slope Compensation**
- **Adjustable Soft-start**
- **LLP-12 (3mm x 3mm)**

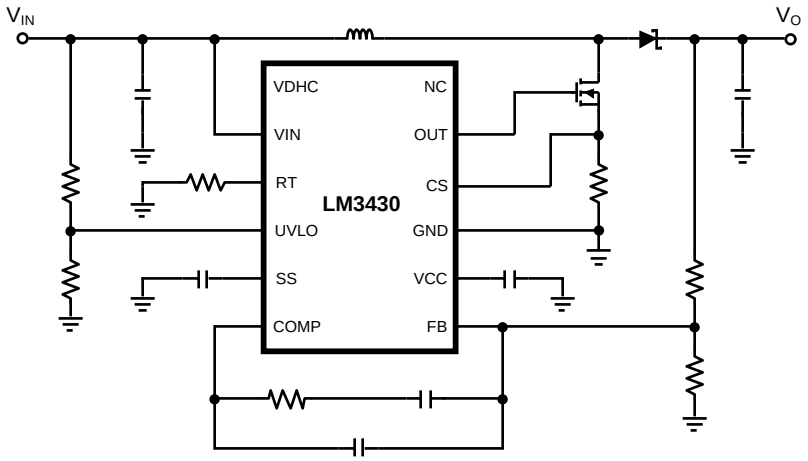
APPLICATIONS

- **LED Backlight Driver (companion to LM3432)**
- **Boost Converter**
- **SEPIC Converter**

DESCRIPTION

The LM3430 is a high voltage low-side N-channel MOSFET controller. Ideal for use in a boost regulator, the LM3430 can power the LED backlight in LCD panels, such as in notebook PCs. It contains all of the features needed to implement single ended primary topologies. Output voltage regulation is based on current-mode control, which eases the design of loop compensation while providing inherent input voltage feed-forward. The LM3430 includes a start-up regulator that operates over a wide input range of 6V to 40V. The PWM controller is designed for high speed capability including an oscillator frequency range up to 2 MHz and total propagation delays less than 100 ns. Additional features include an error amplifier, precision reference, line under-voltage lockout, cycle-by-cycle current limit, slope compensation, soft-start, external synchronization capability and thermal shutdown. The LM3430 is available in the LLP-12 package.

Typical Application



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Connection Diagram

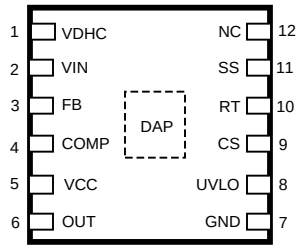

Figure 1. 12-Lead LLP Package

Pin Functions

Pin Descriptions

Pin(s)	Name	Description	Application Information
1	VDHC	Proprietary control input from LM3432	This pin accepts a control signal from LM3432 to adjust the output voltage in real time.
2	VIN	Source input voltage	Input to the start-up regulator. Operates from 6V to 40V.
3	FB	Feedback pin	Inverting input to the internal voltage error amplifier. The non-inverting input of the error amplifier connects to a 1.25V reference.
4	COMP	Error amplifier output and PWM comparator input	The control loop compensation components connect between this pin and the FB pin.
5	VCC	Output of the internal, high voltage linear regulator.	This pin should be bypassed to the GND pin with a ceramic capacitor.
6	OUT	Output of gate driver	Connect this pin to the gate of the external MOSFET. The gate driver has a 1A peak current capability.
7	GND	System ground	
8	UVLO	Input Under-Voltage Lock-out	Set the start-up and shutdown levels by connecting this pin to the input voltage through a resistor divider. A 20 µA current source provides hysteresis.
9	CS	Current Sense input	Input for the switch current sensing used for current mode control and for current limiting.
10	RT/SYNC	Oscillator frequency adjust pin and synchronization input	An external resistor connected from this pin to GND sets the oscillator frequency. This pin can also accept an ac-coupled input for synchronization from an external clock.
11	SS	Soft-start pin	An external capacitor placed from this pin to ground will be charged by a 10 µA current source, creating a ramp voltage to control the regulator start-up.
12	NC	No-connect	Leave this pin open-circuit.
DAP	EP	Exposed Pad	Thermal connection pad, connect to GND.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings [1]

VIN to GND	-0.3V to 45V
VCC to GND	-0.3V to 16V
RT/SYNC to GND	-0.3V to 5.5V
OUT to GND	-1.5V for < 100 ns
All other pins to GND	-0.3V to 7V
Power Dissipation	Internally Limited
Junction Temperature	150°C
Storage Temperature	-65°C to +150°C
Soldering Information	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
ESD Rating	
Human Body Model [2]	2 kV

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. The Recommended Operating Limits define the conditions within which the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.
(2) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin.

Operating Ranges [1]

Supply Voltage	6V to 40V
External Volatge at V_{CC}	7.5V to 14V
Junction Temperature Range	-40°C to +125°C

(1) Device thermal limitations may limit usable range.

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Electrical Characteristics

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. V_{IN} = 18V and R_T = 27.4 kΩ unless otherwise indicated. (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SYSTEM PARAMETERS						
V_{FB}	FB Pin Voltage	-40°C ≤ T_J ≤ 125°C	**1.225**	1.250	**1.275**	V
START-UP REGULATOR						
VCC	VCC Regulation	9V ≤ V_{IN} ≤ 40V, I_{CC} = 1 mA	**6.6**	7	**7.4**	V
	VCC Regulation	6V ≤ V_{IN} < 9V, VCC Pin Open Circuit	**5**			
I_{CC}	Supply Current	OUT Pin Capacitance = 0 VCC = 10V		3.5	**4**	mA
I_{CC-LIM}	VCC Current Limit	VCC = 0V, (Note 4, 6)	**15**	35		mA
V_{IN} - VCC	Dropout Voltage Across Bypass Switch	I_{CC} = 0 mA, f_{SW} < 200 kHz 6V ≤ V_{IN} ≤ 8.5V		200		mV
V_{BYP-HI}	Bypass Switch Turn-off Threshold	V_{IN} increasing		8.7		V
$V_{BYP-HYS}$	Bypass Switch Threshold Hysteresis	V_{IN} Decreasing		260		mV
Z_{VCC}	VCC Pin Output Impedance 0 mA ≤ ICC ≤ 5 mA	V_{IN} = 6.0V		58		Ω
		V_{IN} = 8.0V		53		
		V_{IN} = 18.0V		1.1		
VCC_{-HI}	VCC Pin UVLO Rising Threshold			5		V
VCC_{-HYS}	VCC Pin UVLO Falling Hysteresis			300		mV
I_{VIN}	Start-up Regulator Leakage	V_{IN} = 40V		150	**500**	µA
I_{IN-SD}	Shutdown Current	V_{UVLO} = 0V, VCC = Open Circuit		350	**450**	µA
ERROR AMPLIFIER						
GBW	Gain Bandwidth			4		MHz
A_{DC}	DC Gain			75		dB
I_{COMP}	COMP Pin Current Sink Capability	V_{FB} = 1.5V V_{COMP} = 1V	**5**	17		mA
UVLO						
V_{SD}	Shutdown Threshold		**1.22**	1.25	**1.28**	V
I_{SD-HYS}	Shutdown Hysteresis Current Source		**16**	20	**24**	µA
CURRENT LIMIT						
$t_{LIM-DLY}$	Delay from ILIM to Output	CS steps from 0V to 0.6V OUT transitions to 90% of VCC		30		ns
V_{CS}	Current Limit Threshold Voltage		**0.45**	0.5	**0.55**	V
t_{BLK}	Leading Edge Blanking Time			65		ns
R_{CS}	CS Pin Sink Impedance	Blanking active		40	**75**	Ω
SOFT-START						
I_{SS}	Soft-start Current Source		**7**	10	**13**	µA
V_{SS-OFF}	Soft-start to COMP Offset		**0.35**	0.55	**0.75**	V
OSCILLATOR						
f_{SW}	RT to GND = 84.5 kΩ	(Note 5)	**170**	200	**230**	kHz
	RT to GND = 27.4 kΩ	(Note 5)	**525**	600	**675**	kHz
	RT to GND = 16.2 kΩ	(Note 5)	**865**	990	**1115**	kHz
$V_{SYNC-HI}$	Synchronization Rising Threshold		**3.8**			V
PWM COMPARATOR						
$t_{COMP-DLY}$	Delay from COMP to OUT Transition	V_{COMP} = 2V CS stepped from 0V to 0.4V		25		ns

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Electrical Characteristics (continued)

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. V_{IN} = 18V and R_T = 27.4 kΩ unless otherwise indicated. (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
D_{MIN}	Minimum Duty Cycle	V_{COMP} = 0V			**0**	%
D_{MAX}	Maximum Duty Cycle		**90**	95		%
A_{PWM}	COMP to PWM Comparator Gain			0.33		V/V
$V_{COMP-OC}$	COMP Pin Open Circuit Voltage	V_{FB} = 0V	**4.3**	5.2	**6.1**	V
$I_{COMP-SC}$	COMP Pin Short Circuit Current	V_{COMP} = 0V, V_{FB} = 1.5V	**0.6**	1.1	**1.5**	mA
SLOPE COMPENSATION						
V_{SLOPE}	Slope Compensation Amplitude		**80**	105	**130**	mV
MOSFET DRIVER						
V_{SAT-HI}	Output High Saturation Voltage (VCC – VOUT)	I_{OUT} = 50 mA		0.25	**0.75**	V
V_{SAT-LO}	Output Low Saturation Voltage (VOUT)	I_{OUT} = 100 mA		0.25	**0.75**	V
t_{RISE}	OUT Pin Rise Time	OUT Pin load = 1 nF		18		ns
t_{FALL}	OUT Pin Fall Time	OUT Pin load = 1 nF		15		ns
THERMAL CHARACTERISTICS						
T_{SD}	Thermal Shutdown Threshold			165		°C
T_{SD-HYS}	Thermal Shutdown Hysteresis			25		°C
θ_{JA}	Junction to Ambient Thermal Resistance	SDF-12A Package		122		°C/W

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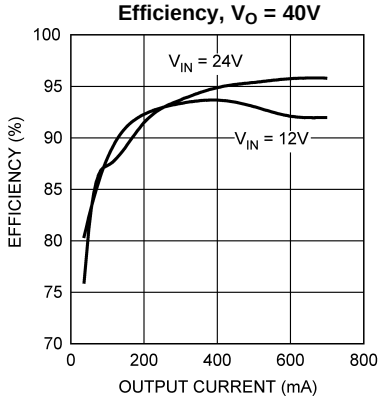
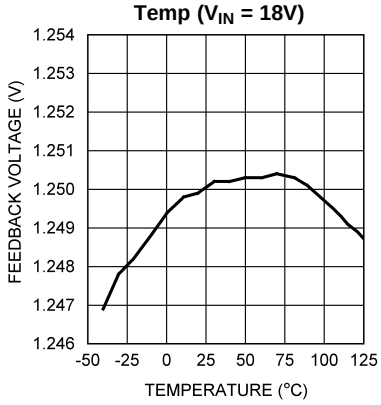
Typical Performance Characteristics

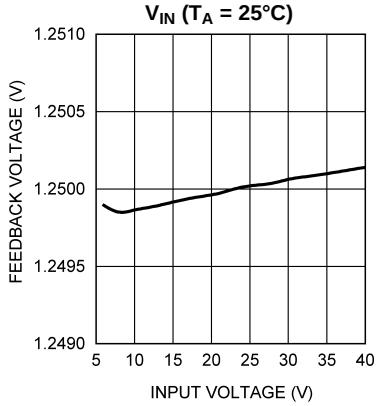
Efficiency, V_O = 40V



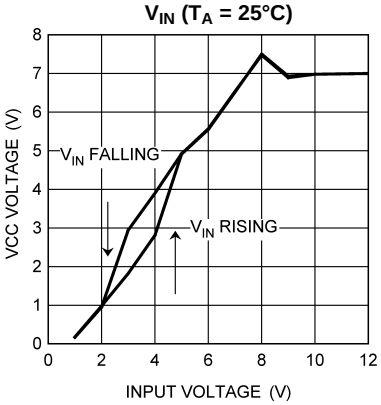
V_{FB} vs. Temp (V_{IN} = 18V)



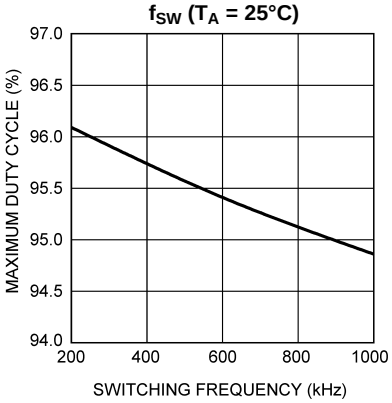
V_{FB} vs. V_{IN} (T_A = 25°C)



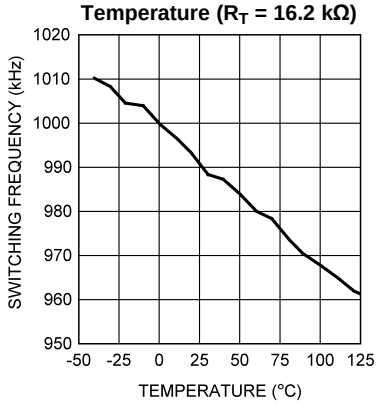
V_{CC} vs. V_{IN} (T_A = 25°C)



Max Duty Cycle vs. f_{SW} (T_A = 25°C)



f_{SW} vs. Temperature (R_T = 16.2 kΩ)



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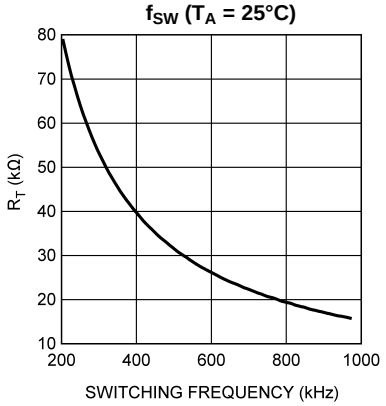
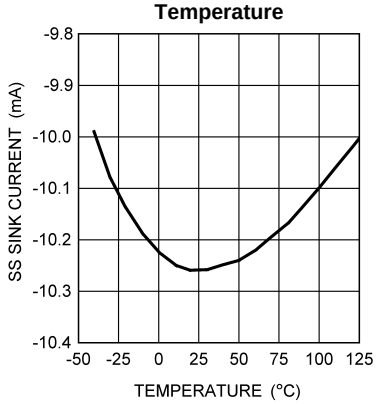
Typical Performance Characteristics (continued)

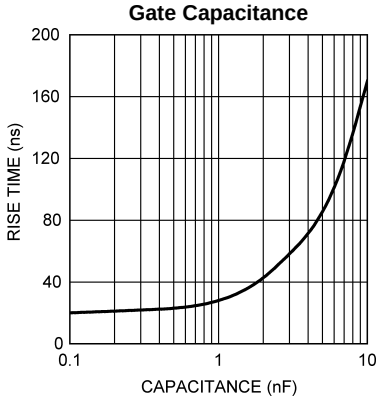
R_T vs. f_{SW} (T_A = 25°C)



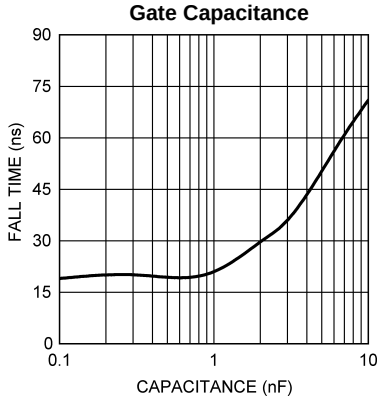
SS vs. Temperature



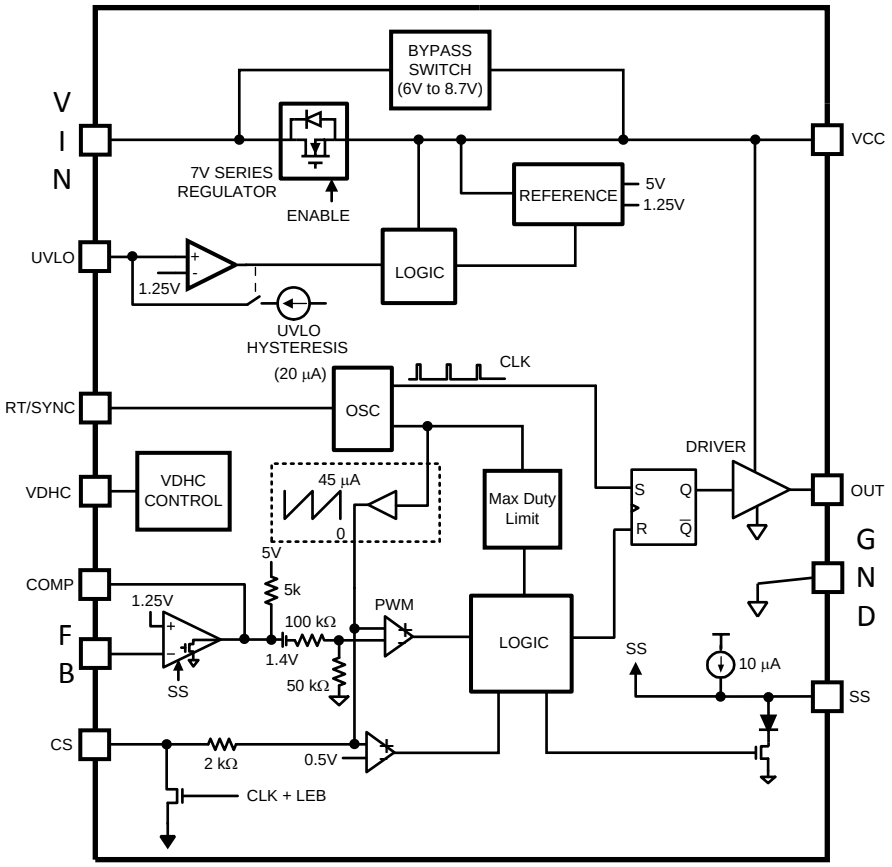
OUT Pin t_R vs. Gate Capacitance



OUT Pin t_F vs. Gate Capacitance



Block Diagram



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Example Circuit: LM3430 and LM3432

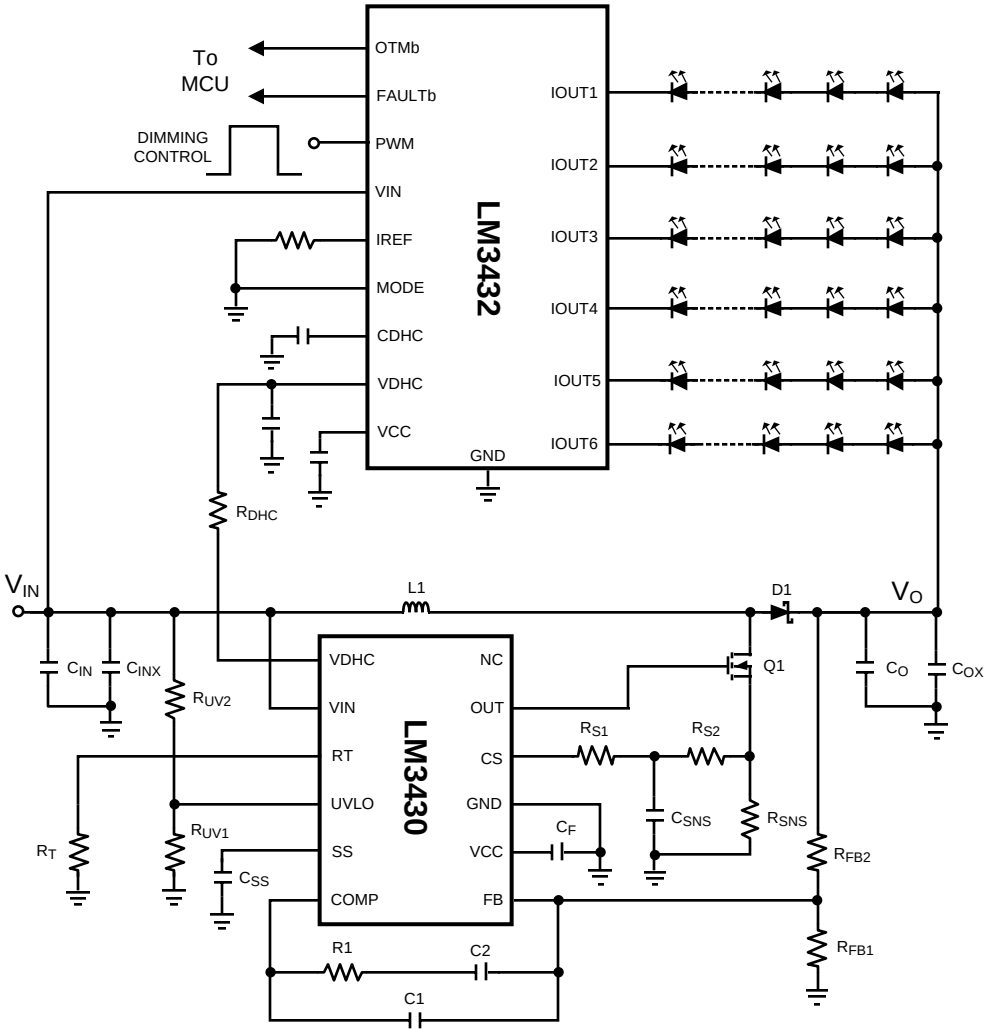

Figure 2. LM3430 with LM3432

Application Parameters for Various LED Configurations

Input Voltage	8V to 21V	8V to 21V	8V to 18V
Maximum Output Voltage	33V	50V	33V
LED Configuration	8 LEDs x 6 Strings, 20 mA per string	12 LEDs x 6 Strings, 20 mA per string	8 LEDs x 6 Strings, 20 mA per string
Switching Frequency	1 MHz	1 MHz	2 MHz
L1	22 µH	22 µH	4.7 µH
Co	10 µF, 50V	20 µF, 100V	10 µF, 50V
Cin	10 µF, 50V	10 µF, 50V	10 µF, 50V
Cinx	100 nF	100 nF	100 nF
Css	1 nF	1 nF	1 nF
Rt	16.5 kΩ	16.5 kΩ	8.25 kΩ
Rfb1	4.64 kΩ	3.01 kΩ	16.5 kΩ
Rfb2	118 kΩ	118 kΩ	422 kΩ

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Ruv1	10 kΩ	10 kΩ	10 kΩ
Ruv2	49.9 kΩ	49.9 kΩ	49.9 kΩ
Control Loop Compensation			
C1	12 pF	12 pF	39 pF
R1	75 kΩ	118 kΩ	150 kΩ
C2	220 nF	47 nF	4.7 nF
VDHC			
Rdhc	30 kΩ	9.09 kΩ	60.4 kΩ
Slope Compensation			
Rs1	4.02 kΩ	4.02 kΩ	4.02 kΩ
Rs2	301Ω	301Ω	301Ω
Current Sensing			
Rsns	0.2Ω (1W)	0.2Ω (1W)	Two 1Ω (1W) in parallel
Csns	1 nF	1 nF	1 nF

Applications Information

OVERVIEW

The LM3430 is a low-side N-channel MOSFET controller that contains all of the features needed to implement single ended power converter topologies. The LM3430 includes a high-voltage startup regulator that operates over a wide input range of 6V to 40V. The PWM controller is designed for high speed capability including an oscillator frequency range up to 2 MHz and total propagation delays less than 100 ns. Additional features include an error amplifier, precision reference, input under-voltage lockout, cycle-by-cycle current limit, slope compensation, soft-start, oscillator sync capability and thermal shutdown.

The LM3430 is designed for current-mode control power converters that require a single drive output, such as boost and SEPIC topologies. The LM3430 provides all of the advantages of current-mode control including input voltage feed-forward, cycle-by-cycle current limiting and simplified loop compensation.

HIGH VOLTAGE START-UP REGULATOR

The LM3430 contains an internal high-voltage startup regulator that allows the VIN pin to be connected directly to line voltages as high as 40V. The regulator output is internally current limited to 35 mA (typical). When power is applied, the regulator is enabled and sources current into an external capacitor, C_F, connected to the VCC pin. The recommended capacitance range for C_F is 0.1 µF to 100 µF. When the voltage on the VCC pin reaches the rising threshold of 5V, the controller output is enabled. The controller will remain enabled until VCC falls below 4.7V. In applications using a transformer, an auxiliary winding can be connected through a diode to the VCC pin. This winding should raise the VCC pin voltage to above 7.5V to shut off the internal startup regulator. Powering VCC from an auxiliary winding improves conversion efficiency while reducing the power dissipated in the controller. The capacitance of C_F must be high enough that the it maintains the VCC voltage greater than the VCC UVLO falling threshold (4.7V) during the initial start-up. During a fault condition when the converter auxiliary winding is inactive, external current draw on the VCC line should be limited such that the power dissipated in the start-up regulator does not exceed the maximum power dissipation capability of the controller.

An external start-up or other bias rail can be used instead of the internal start-up regulator by connecting the VCC and the VIN pins together and feeding the external bias voltage (7.5V to 14V) to the two pins.

INPUT UNDER-VOLTAGE DETECTOR

The LM3430 contains an input Under Voltage Lock Out (UVLO) circuit. UVLO is programmed by connecting the UVLO pin to the center point of an external voltage divider from VIN to GND. The resistor divider must be designed such that the voltage at the UVLO pin is greater than 1.25V when VIN is in the desired operating range. If the under voltage threshold is not met, all functions of the controller are disabled and the controller remains in a low power standby state. UVLO hysteresis is accomplished with an internal 20 µA current source

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that is switched on or off into the impedance of the set-point divider. When the UVLO threshold is exceeded, the current source is activated to instantly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 1.25V threshold the current source is turned off, causing the voltage at the UVLO pin to fall. The UVLO pin can also be used to implement a remote enable / disable function. If an external transistor pulls the UVLO pin below the 1.25V threshold, the converter will be disabled. This external shutdown method is shown in Figure 3.

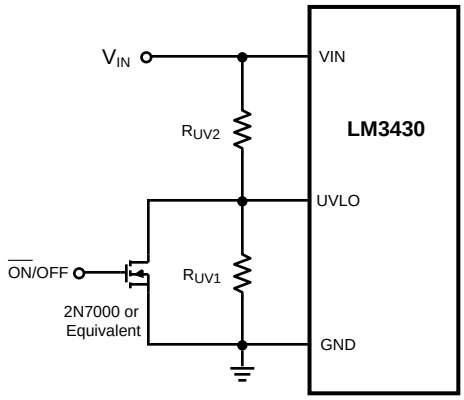

Figure 3. Enable/Disable Using UVLO

ERROR AMPLIFIER

An internal high gain error amplifier is provided within the LM3430. The amplifier's non-inverting input is internally set to a fixed reference voltage of 1.25V. The inverting input is connected to the FB pin. In non-isolated applications such as the boost converter the output voltage, V_O, is connected to the FB pin through a resistor divider. The control loop compensation components are connected between the COMP and FB pins. For most isolated applications the error amplifier function is implemented on the secondary side of the converter and the internal error amplifier is not used. The internal error amplifier is configured as an open drain output and can be disabled by connecting the FB pin to ground. An internal 5 kΩ pull-up resistor between a 5V reference and COMP can be used as the pull-up for an opto-coupler in isolated applications.

CURRENT SENSING AND CURRENT LIMITING

The LM3430 provides a cycle-by-cycle over current protection function. Current limit is accomplished by an internal current sense comparator. If the voltage at the current sense comparator input exceeds 0.5V, the MOSFET gate drive will be immediately terminated. A small RC filter, located near the controller, is recommended to filter noise from the current sense signal. The CS input has an internal MOSFET which discharges the CS pin capacitance at the conclusion of every cycle. The discharge device remains on an additional 65 ns after the beginning of the new cycle to attenuate leading edge ringing on the current sense signal.

The LM3430 current sense and PWM comparators are very fast, and may respond to short duration noise pulses. Layout considerations are critical for the current sense filter and sense resistor. The capacitor associated with the CS filter must be located very close to the device and connected directly to the pins of the controller (CS and GND). If a current sense transformer is used, both leads of the transformer secondary should be routed to the sense resistor and the current sense filter network. The current sense resistor can be located between the source of the primary power MOSFET and power ground, but it must be a low inductance type. When designing with a current sense resistor all of the noise sensitive low-power ground connections should be connected together locally to the controller and a single connection should be made to the high current power ground (sense resistor ground point).

OSCILLATOR, SHUTDOWN AND SYNC

A single external resistor, R_T, connected between the RT/SYNC and GND pins sets the LM3430 oscillator frequency. To set the switching frequency, f_{SW}, R_T can be calculated from:

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$$R_T = \frac{1 - 8 \times 10^{-8} \times f_{SW}}{f_{SW} \times 5.77 \times 10^{-11}} \quad (f_{SW} \text{ in Hz, } R_T \text{ in } \Omega) \tag{1}$$

The LM3430 can also be synchronized to an external clock. The external clock must have a higher frequency than the free running oscillator frequency set by the R_T resistor. The clock signal should be capacitively coupled into the RT/SYNC pin with a 100 pF capacitor, shown in Figure 4. A peak voltage level greater than 3.8V at the RT/SYNC pin is required for detection of the sync pulse. The sync pulse width should be set between 15 ns to 150 ns by the external components. The R_T resistor is always required, whether the oscillator is free running or externally synchronized. The voltage at the RT/SYNC pin is internally regulated to 2V, and the typical delay from a logic high at the RT/SYNC pin to the rise of the OUT pin voltage is 120 ns. R_T should be located very close to the device and connected directly to the pins of the controller (RT/SYNC and GND).

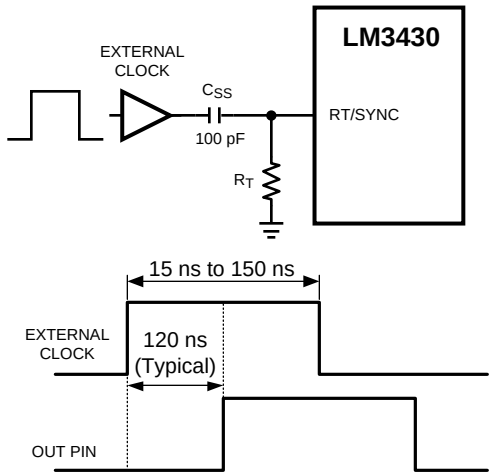

Figure 4. Sync Operation

PWM COMPARATOR AND SLOPE COMPENSATION

The PWM comparator compares the current ramp signal with the error voltage derived from the error amplifier output. The error amplifier output voltage at the COMP pin is offset by 1.4V and then further attenuated by a 3:1 resistor divider. The PWM comparator polarity is such that 0V on the COMP pin will result in a zero duty cycle at the controller output. For duty cycles greater than 50%, current mode control circuits can experience sub-harmonic oscillation. By adding an additional fixed-slope voltage ramp signal (slope compensation) this oscillation can be avoided. The LM3430 generates the slope compensation with a 45 μA_{P-P} sawtooth-waveform current source generated by the clock. (See Figure 5) This current flows through an internal 2 kΩ resistor to create a minimum compensation ramp voltage of 100 mV (typical). The amplitude of the compensation ramp increases when external resistance is added for filtering the current sense (R_{S1}) or in the position R_{S2}. As shown in Figure 5 and the block diagram, the sensed current slope and the compensation slope add together to create the signal used for current limiting and for the control loop itself.

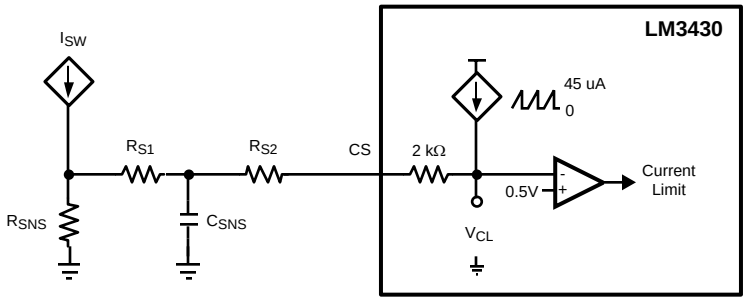

Figure 5. Slope Compensation

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In addition to preventing sub-harmonic oscillation, increasing the amplitude of the compensation ramp voltage decreases the voltage across R_{SNS} required to trip the current limit comparator. This technique can be used to lower the value of R_{SNS} and reduce power dissipation. Care must be taken not to add too much slope compensation, however. Reducing R_{SNS} causes the control loop gain to increase, and too large of a compensation ramp can overwhelm the sensed current signal. This imbalance causes the system to act more like a voltage-mode regulator with a low frequency double pole that is more difficult to compensate.

SOFT-START

The soft-start feature allows the power converter output to gradually reach the initial steady state output voltage, thereby reducing start-up stresses and current surges. At power on, after the VCC and input under-voltage lockout thresholds are satisfied, an internal 10 µA current source charges an external capacitor connected to the SS pin. The capacitor voltage will ramp up slowly and will limit the COMP pin voltage and the switch current.

MOSFET GATE DRIVER

The LM3430 provides an internal gate driver through the OUT pin that can source and sink a peak current of 1A to control external, ground-referenced MOSFETs.

DYNAMIC HEADROOM CONTROL

The VDHC pin of the LM3430 can be used in conjunction with the LM3432 to provide on-the-fly adjustments to the output voltage for maximum efficiency when driving an array of LEDs. When this feature is not being used the VDHC pin should be left open circuit.

THERMAL SHUTDOWN

Internal thermal shutdown circuitry is provided to protect the LM3430 in the event that the maximum junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low power standby state, disabling the output driver and the VCC regulator. After the temperature is reduced (typical hysteresis is 25°C) the VCC regulator will be re-enabled and the LM3430 will perform a soft-start.

Design Considerations

The most common circuit controlled by the LM3430 is a non-isolated boost regulator. The boost regulator steps up the input voltage and has a duty ratio D of:

$$D = \frac{V_O - V_{IN} - V_D}{V_O - V_D} \quad (V_D \text{ is the forward voltage drop of the output diode}) \tag{2}$$

The following is a design procedure for selecting all the components for the boost converter portion of the Example Circuit of Figure 2. This circuit operates in continuous conduction mode (CCM), where inductor current stays above 0A at all times, and delivers an output voltage of 33.0V ±2% at an output current of 180 mA. The load is a white LED-based LCD monitor backlight, formed by six parallel strings of seven white LEDs each with a multi-channel linear current regulator to sink 30 mA through each string. The forward voltage of each LED varies from 3.0V to 4.2V over process and temperature and the current regulator requires approximately 4V of headroom. The required output voltage is therefore 7 x 4.2V + 4V ≅ 33V.

The input voltage will come from a three-to-four-cell stack of lithium ion batteries (V_{IN} = 9.0V to 16.8V) or a poorly regulated AC-DC adapter that supplies 14.0V to 20.9V. The diode drop V_D will be 0.5V, typical of a Schottky diode.

SWITCHING FREQUENCY

The selection of switching frequency is based on the tradeoffs between size, cost, and efficiency. In general, a lower frequency means larger, more expensive inductors and capacitors will be needed. A higher switching frequency generally results in a smaller but less efficient solution, as the power MOSFET gate capacitances must be charged and discharged more often in a given amount of time. For this application, a frequency of 600 kHz was selected as a good compromise between the size of the inductor and efficiency. PCB area and component height are restricted in this application. Following the equation given for RT in the Applications Information section, a 27.4 kΩ 1% resistor should be used to switch at 600 kHz.

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MOSFET

Selection of the power MOSFET is governed by tradeoffs between cost, size, and efficiency. Breaking down the losses in the MOSFET is one way to determine relative efficiencies between different devices. For this example, the SO-8 package provides a balance of a small footprint with good efficiency.

Losses in the MOSFET can be broken down into conduction loss, gate charging loss, and switching loss.

Conduction, or I^2R loss, P_C, is approximately:

$$P_C = D \times \left[\left(\frac{I_O}{1-D}\right)^2 \times R_{DSON} \times 1.3\right] \tag{3}$$

The factor 1.3 accounts for the increase in MOSFET on resistance due to heating. Alternatively, the factor of 1.3 can be ignored and the on resistance of the MOSFET can be estimated using the R_{DSON} Vs. Temperature curves in the MOSFET datasheets.

Gate charging loss, P_G, results from the current required to charge and discharge the gate capacitance of the power MOSFET and is approximated as:

$$P_G = VCC \times Q_G \times f_{SW} \tag{4}$$

Q_G is the total gate charge of the MOSFET. Gate charge loss differs from conduction and switching losses because the actual dissipation occurs in the LM3430 and not in the MOSFET itself. If no external bias is applied to the VCC pin, additional loss in the LM3430 IC occurs as the MOSFET driving current flows through the VCC regulator. This loss, P_{VCC}, is estimated as:

$$P_{VCC} = (V_{IN} - VCC) \times Q_G \times f_{SW} \tag{5}$$

Switching loss, P_{SW}, occurs during the brief transition period as the MOSFET turns on and off. During the transition period both current and voltage are present in the channel of the MOSFET. The loss can be approximated as:

$$P_{SW} = 0.5 \times V_{IN} \times [I_O / (1 - D)] \times (t_R + t_F) \times f_{SW} \tag{6}$$

Where t_R and t_F are the rise and fall times of the MOSFET

For this example, the maximum drain-to-source voltage applied across the MOSFET is V_O plus the ringing due to parasitic inductance and capacitance. The maximum drive voltage at the gate of the high side MOSFET is VCC, or 7V typical. The MOSFET selected must be able to withstand 33V plus any ringing from drain to source, and be able to handle at least 7V plus ringing from gate to source. A minimum voltage rating of 40VD-S and 10VG-S MOSFET will be used. Comparing the losses in a spreadsheet leads to a 60VD-S rated MOSFET in SO-8 with a typical R_{DSON} of 22 mΩ, a gate charge of 18 nC, and rise and falls times of 10 ns and 12 ns, respectively.

BOOST DIODE

The boost regulator requires a boost diode D1 (see the Typical Application circuit) to carrying the inductor current during the MOSFET off-time. The most efficient choice for D1 is a Schottky diode due to low forward drop and zero reverse recovery time. D1 must be rated to handle the maximum output voltage plus any switching node ringing when the MOSFET is on. In practice, all switching converters have some ringing at the switching node due to the diode parasitic capacitance and the lead inductance. D1 must also be rated to handle the average output current, I_O.

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The overall converter efficiency becomes more dependent on the selection of D1 at low duty cycles, where the boost diode carries the load current for an increasing percentage of the time. This power dissipation can be calculating by checking the typical diode forward voltage, V_D, from the I-V curve on the diode's datasheet and then multiplying it by I_D. Diode datasheets will also provide a typical junction-to-ambient thermal resistance, θ_{JA}, which can be used to estimate the operating die temperature of the Schottky. Multiplying the power dissipation ($P_D = I_O \times V_D$) by θ_{JA} gives the temperature rise. The diode case size can then be selected to maintain the Schottky diode temperature below the operational maximum.

In this example a Schottky diode rated to 40V and 0.5A will be suitable, as the maximum diode current will be 180 mA. A small case such as SOD-123 or SOT-23 can be used if a small footprint is critical. Larger case sizes generally have lower θ_{JA} and lower forward voltage drop, so for better efficiency, a larger case size such as SMA can be used. In applications with a high boost ratio, such as 1:4, the reverse recovery time, t_{RR}, has a large impact on losses and efficiency. The Schottky diode selected should therefore have a t_{RR} value below 15 ns.

BOOST INDUCTOR

The first criterion for selecting an inductor is the inductance itself. In fixed-frequency boost converters this value is based on the desired peak-to-peak ripple current, Δi_L, which flows in the inductor along with the average inductor current, I_L. For a boost converter in CCM I_L is greater than the average output current, I_O. The two currents are related by the following expression:

$$I_L = I_O / (1 - D) \tag{7}$$

As with switching frequency, the inductance used is a tradeoff between size and cost. Larger inductance means lower input ripple current, however because the inductor is connected to the output during the off-time only there is a limit to the reduction in output ripple voltage. Lower inductance results in smaller, less expensive magnetics. An inductance that gives a ripple current of 30% to 50% of I_L is a good starting point for a CCM boost converter. Minimum inductance should be calculated at the extremes of input voltage to find the operating condition with the highest requirement:

$$L_1 = \frac{V_{IN} \times D}{f_{SW} \times \Delta i_L} \tag{8}$$

By calculating in terms of amperes, volts, and megahertz, the inductance value will come out in microhenrys.

In order to ensure that the boost regulator operates in CCM a second equation is needed, and must also be evaluated at the corners of input voltage to find the minimum inductance required:

$$L_2 = \frac{D(1-D) \times V_{IN}}{I_O \times f_{SW}} \tag{9}$$

By calculating in terms of volts, amps and megahertz the inductance value will come out in microhenrys.

For this design Δi_L will be set to 40% of the maximum I_L. Duty cycle is evaluated first at $V_{IN(MIN)}$ and at $V_{IN(MAX)}$. Second, the average inductor current is evaluated at the two input voltages. Third, the inductor ripple current is determined. Finally, the inductance can be calculated, and a standard inductor value selected that meets all the criteria.

Inductance for Minimum Input Voltage

$$D_{VIN(MIN)} = (33 - 9.0 - 0.5) / (33 - 0.5) = 72\% \quad I_{L\text{-}VIN(MIN)} = 0.18 / (1 - 0.72) = 0.64A \quad \Delta i_L = 0.4 \times 0.64A = 0.26A \tag{10}$$

$$L_{1\text{-}VIN(MIN)} = \frac{9 \times 0.72}{0.6 \times 0.26} = 42\ \mu H \tag{11}$$

$$L_{2\text{-}VIN(MIN)} = \frac{0.72 \times 0.28 \times 9}{0.18 \times 0.6} = 17\ \mu H \tag{12}$$

Inductance for Maximum Input Voltage

$$D_{VIN(MAX)} = (33 - 20.9) / 33 = 37\% \quad I_{L\text{-}VIN(MIAX)} = 0.18 / (1 - 0.37) = 0.29A \quad \Delta i_L = 0.4 \times 0.29A = 0.12A \tag{13}$$

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$$L_{1\text{-}VIN(MAX)} = \frac{20.9 \times 0.36}{0.6 \times 0.12} = 105\ \mu H \quad (14)$$

$$L_{2\text{-}VIN(MAX)} = \frac{0.36 \times 0.64 \times 20.9}{0.18 \times 0.6} = 45\ \mu H \quad (15)$$

Maximum average inductor current occurs at $V_{IN(MIN)}$, and the corresponding inductor ripple current is $0.26A_{P\text{-}P}$. Selecting an inductance that exceeds the ripple current requirement at $V_{IN(MIN)}$ and the requirement to stay in CCM for $V_{IN(MAX)}$ provides a tradeoff that allows smaller magnetics at the cost of higher ripple current at maximum input voltage. For this example, a 47 µH inductor will satisfy these requirements.

The second criterion for selecting an inductor is the peak current carrying capability. This is the level above which the inductor will saturate. In saturation the inductance can drop off severely, resulting in higher peak current that may overheat the inductor or push the converter into current limit. In a boost converter, peak current, I_{PK}, is equal to the maximum average inductor current plus one half of the ripple current. First, the current ripple must be determined under the conditions that give maximum average inductor current:

$$\Delta i_L = \frac{V_{IN} \times D}{f_{SW} \times L} \quad (16)$$

Maximum average inductor current occurs at $V_{IN(MIN)}$. Using the selected inductance of 47 µH yields the following:

$$\Delta i_L = (9 \times 0.72) / (0.6 \times 47) = 230\ mA_{P\text{-}P} \quad (17)$$

The highest peak inductor current over all operating conditions is therefore:

$$I_{PK} = I_L + 0.5 \times \Delta i_L = 0.64 + 0.115 = 0.76A \quad (18)$$

Hence an inductor must be selected that has a peak current rating greater than 0.76A and an average current rating greater than 0.64A. One possibility is an off-the-shelf 47 µH ±20% inductor that can handle a peak current of 0.9A and an average current of 0.93A. Finally, the inductor current ripple is recalculated at the maximum input voltage:

$$\Delta i_{L\text{-}VIN(MAX)} = (20.9 \times 0.36) / (0.6 \times 47) = 267\ mA_{P\text{-}P} \quad (19)$$

OUTPUT CAPACITOR

The output capacitor in a boost regulator supplies current to the load during the MOSFET on-time and also filters the AC portion of the load current during the off-time. This capacitor determines the steady state output voltage ripple, ΔV_O, a critical parameter for all voltage regulators. Output capacitors are selected based on their capacitance, C_O, their equivalent series resistance (ESR) and their RMS or AC current rating.

The magnitude of ΔV_O is comprised of three parts, and in steady state the ripple voltage during the on-time is equal to the ripple voltage during the off-time. For simplicity the analysis will be performed for the MOSFET turning off (off-time) only. The first part of the ripple voltage is the surge created as the output diode D1 turns on. At this point inductor/diode current is at the peak value, and the ripple voltage increase can be calculated as:

$$\Delta V_{O1} = I_{PK} \times ESR \quad (20)$$

The second portion of the ripple voltage is the increase due to the charging of C_O through the output diode. This portion can be approximated as:

$$\Delta V_{O2} = (I_O / C_O) \times (D / f_{SW}) \quad (21)$$

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The final portion of the ripple voltage is a decrease due to the flow of the diode/inductor current through the output capacitor's ESR. This decrease can be calculated as:

$$\Delta V_{O3} = \Delta i_L \times ESR \tag{22}$$

The total change in output voltage is then:

$$\Delta V_O = \Delta V_{O1} + \Delta V_{O2} - \Delta V_{O3} \tag{23}$$

The combination of two positive terms and one negative term may yield an output voltage ripple with a net rise or a net fall during the converter off-time. The ESR of the output capacitor(s) has a strong influence on the slope and direction of ΔV_O. Capacitors with high ESR such as tantalum and aluminum electrolytic create an output voltage ripple that is dominated by ΔV_{O1} and ΔV_{O3}, with a shape shown in Figure 6. Ceramic capacitors, in contrast, have very low ESR and lower capacitance. The shape of the output ripple voltage is dominated by ΔV_{O2}, with a shape shown in Figure 7.

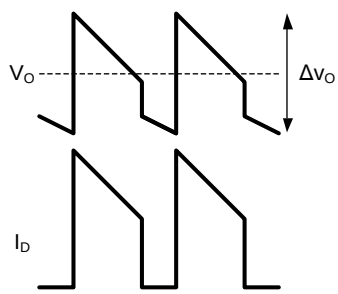

Figure 6. ΔV_O Using High ESR Capacitors

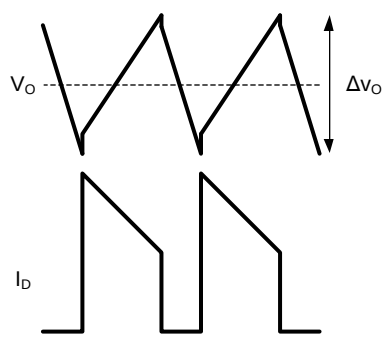

Figure 7. ΔV_O Using Low ESR Capacitors

For this example, the load is fairly constant, and the height restriction favors the low profile of ceramic capacitors. The output ripple voltage waveform of Figure 7 is assumed, and the capacitance will be selected first. The desired ΔV_O is ±2% of 33V, or $1.32V_{P-P}$. Beginning with the calculation for ΔV_{O2}, the required minimum capacitance is:

$$C_{O\text{-}MIN} = (I_O / \Delta V_O) \times (D_{MAX} / f_{SW})\ C_{O\text{-}MIN} = (0.18 / 1.32) \times (0.72 / 600000) = 164\ nF \tag{24}$$

Ceramic capacitors rated 1.0 µF ±20% are available from many manufacturers. The minimum quality dielectric that is suitable for switching power supply output capacitors is X5R, while X7R (or better) is preferred. Careful attention must be paid to the DC voltage rating and case size, as ceramic capacitors can lose 60%+ of their rated capacitance at the maximum DC voltage. For example, the typical loss in capacitance for a 1.0 µF, 50V, 1206-size capacitor is 50% at 30V. This is the reason that ceramic capacitors are often de-rated to 50% of their capacitance at their working voltage.

The ESR of the selected capacitor has a typical value of 3 mΩ. The worst-case value for ΔV_{O1} occurs during the peak current at minimum input voltage:

$$\Delta V_{O1} = 1.26 \times 0.003 = 3.8 \text{ mV} \tag{25}$$

The worst-case capacitor charging ripple occurs at maximum duty cycle, taking into account an output capacitance of 50% x 1 µF = 500 nF:

$$\Delta V_{O2} = (0.18 / 5 \times 10^{-7}) \times (0.72 / 600000) = 432 \text{ mV} \tag{26}$$

Finally, the worst-case value for ΔV_{O3} occurs when inductor ripple current is highest, at maximum input voltage:

$$\Delta V_{O3} = 0.398 \times 0.003 = 1.2 \text{ mV (negligible)} \tag{27}$$

The output voltage ripple can be estimated by summing the three terms:

$$\Delta V_{O} = 3.8 \text{ mV} + 432 \text{ mV} - 1.2 \text{ mV} = 435 \text{ mV} \tag{28}$$

The RMS current through the output capacitor(s) can be estimated using the following, worst-case equation:

$$I_{O\text{-}RMS} = 1.13 \times I_L \times \sqrt{D \times (1 - D)} \tag{29}$$

The highest RMS current occurs at minimum input voltage. For this example the maximum output capacitor RMS current is:

$$I_{O\text{-}RMS(MAX)} = 1.13 \times 0.64 \times (0.72 \times 0.28)^{0.5} = 0.32A_{RMS} \tag{30}$$

Ceramic capacitors in 1206 case sizes are generally capable of sustaining RMS currents in excess of 2A, making them more than adequate for this application.

VCC DECOUPLING CAPACITOR

The VCC pin should be decoupled with a ceramic capacitor placed as close as possible to the VCC and GND pins of the LM3430. The decoupling capacitor should have a minimum X5R or X7R type dielectric to ensure that the capacitance remains stable over voltage and temperature, and be rated to a minimum of 470 nF. One good choice is a 1.0 µF device with X7R dielectric and 1206 case size rated to 25V.

INPUT CAPACITOR

The input capacitors to a boost regulator control the input voltage ripple, ΔV_{IN}, hold up the input voltage during load transients, and prevent impedance mismatch (also called power supply interaction) between the LM3430 and the inductance of the input leads. Selection of input capacitors is based on their capacitance, ESR, and RMS current rating. The minimum value of ESR can be selected based on the maximum output current transient, I_{STEP}, using the following expression:

$$ESR_{MIN} = \frac{(1\text{-}D) \times \Delta v_{IN}}{2 \times I_{STEP}} \tag{31}$$

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For this example, no specific load transient is given, hence I_{STEP} is set equal to the maximum load current of 180 mA. The desired ΔV_{IN} is $4\%_{P-P}$. ΔV_{IN} and duty cycle are taken at minimum input voltage to give the worst-case value:

$$ESR_{MIN} = [(1 - 0.72) \times 0.36] / 0.36 = 0.28\Omega \tag{32}$$

The minimum input capacitance can be selected based on ΔV_{IN}, based on the drop in V_{IN} during a load transient, or based on prevention of power supply interaction. In general, the requirement for greatest capacitance comes from the power supply interaction. The inductance and resistance of the input source must be estimated, and if this information is not available, they can be assumed to be 1 µH and 0.1Ω, respectively. Minimum capacitance is then estimated as:

$$C_{MIN} = \frac{2 \times L_S \times V_O \times I_O}{V^2_{IN} \times R_S} \tag{33}$$

As with ESR, the worst-case, highest minimum capacitance calculation comes at the minimum input voltage. Using the default estimates for L_S and R_S, minimum capacitance is:

$$C_{MIN} = \frac{2 \times 1 \times 33 \times 0.18}{9^2 \times 0.1} = 1.5\ \mu F \tag{34}$$

The closest standard 20% capacitor value is 1.5 µF, but because the actual input source impedance and resistance are not known, a 3.3 µF capacitor will be used. In general, doubling the calculated value of input capacitance provides a good safety margin. The final calculation is for the RMS current. For boost converters operating in CCM this can be estimated as:

$$I_{RMS} = 0.29 \times \Delta i_{L(MAX)} \tag{35}$$

From the inductor section, maximum inductor ripple current is 267 mA, hence the input capacitor(s) must be rated to handle 0.29 x 0.267 = 77 mA_{RMS}.

The input capacitors can be ceramic, tantalum, aluminum, or almost any type, however the low capacitance requirement makes ceramic capacitors particularly attractive. As with the output capacitors, the minimum quality dielectric used should X5R, with X7R or better preferred. The voltage rating for input capacitors need not be as conservative as the output capacitors, as the need for capacitance decreases as input voltage increases. For this example, the capacitor selected will be 3.3 µF ±20%, rated to 25V, in a 1206 case size. The RMS current rating is over 1A, more than enough for this application.

CURRENT SENSE FILTER

Parasitic circuit capacitance, inductance and gate drive current create a spike in the current sense voltage at the point where Q1 turns on. In order to prevent this spike from terminating the on-time prematurely, every circuit should have a low-pass filter that consists of C_{CS} and R_{S1}, shown in Figure 2. The time constant of this filter should be long enough to reduce the parasitic spike without significantly affecting the shape of the actual current sense voltage. The recommended range for R_{S1} is between 10Ω and 500Ω, and the recommended range for C_{CS} is between 100 pF and 2.2 nF. For this example, the values of R_{S1} and C_{CS} will be 100Ω and 1 nF, respectively.

R_{SNS} AND CURRENT LIMIT

The current sensing resistor R_{SNS} is used for steady state regulation of the inductor current and to sense over-current conditions. The resistance value selected must be low enough to keep the power dissipation to a minimum, yet high enough to provide good signal-to-noise ratio for the current sensing circuitry. The resistance should be set so that the current limit comparator, with a threshold of 0.5V, trips before the sensed current exceeds the peak current rating of the inductor.

For this example the inductor peak current rating is 0.9A. The threshold for current limit, I_{LIM}, is set slightly below to account for tolerance of the circuit components, at a level of 0.8A. The required resistor calculation must take into account both the switch current through R_{SNS} and the compensation ramp current flowing through the internal 2 kΩ and external 100Ω resistors:

$$R_{SNS} = \frac{V_{CS} - 45\ \mu A \times (2\ k\Omega + R_{S1} + R_{S2})}{I_{LIM}} \quad (36)$$

$$R_{SNS} = [0.5 - 45\mu \times (2000 + 100)] / 0.8 = 0.51\Omega \quad (37)$$

Power dissipation in R_{SNS} can be estimated by calculating the average current. The worst-case average current through R_{SNS} occurs at minimum input voltage/maximum duty cycle and can be calculated as:

$$P_{CS} = \left[\left(\frac{I_O}{1-D}\right)^2 \times R_{SNS}\right] \times D \quad (38)$$

$$P_{CS} = [(0.18 / 0.27)^2 \times 0.51] \times 0.73 = 0.16W \quad (39)$$

For this example a 0.51Ω ±1%, thick-film chip resistor in a 1206 case size rated to 0.33W will be used.

CONTROL LOOP COMPENSATION

The LM3430 uses peak current-mode PWM control to correct changes in output voltage due to line and load transients. Peak current-mode provides inherent cycle-by-cycle current limiting, improved line transient response, and easier control loop compensation.

The control loop is comprised of two parts. The first is the power stage, which consists of the pulse width modulator, output filter, and the load. The second part is the error amplifier, which is an op-amp configured as an inverting amplifier. Figure 8 shows the regulator control loop components.

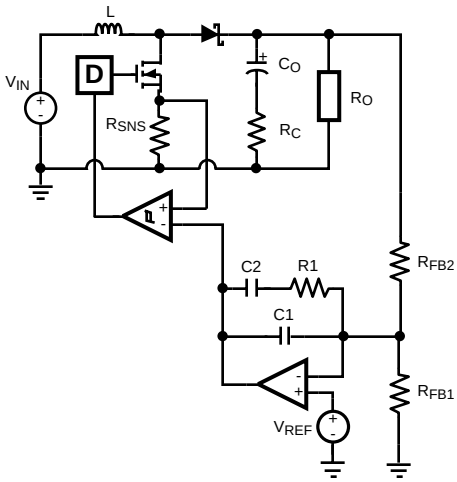

Figure 8. Power Stage and Error Amp

One popular method for selecting the compensation components is to create Bode plots of gain and phase for the power stage and error amplifier. Combined, they make the overall bandwidth and phase margin of the regulator easy to determine. Software tools such as Excel, MathCAD, and Matlab are useful for observing how changes in compensation or the power stage affect system gain and phase.

The power stage in a CCM peak current mode boost converter consists of the DC gain, A_{PS}, a single low frequency pole, f_{LFP}, the ESR zero, f_{ZESR}, a right-half plane zero, f_{RHP}, and a double pole resulting from the sampling of the peak current. The power stage transfer function (also called the Control-to-Output transfer function) can be written:

$$G_{PS} = A_{PS} \times \frac{\left(1 + \frac{s}{\omega_{ZESR}}\right)\left(1 - \frac{s}{\omega_{RHP}}\right)}{\left(1 + \frac{s}{\omega_{LEP}}\right)\left(1 + \frac{s}{Q_n \times \omega_n} + \frac{s^2}{\omega_n^2}\right)} \quad (40)$$

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Where the DC gain is defined as:

$$A_{PS} = \frac{(1 - D) \times R_O}{2 \times R_{SNS}} \tag{41}$$

Where:

$$R_O = V_O / I_O \tag{42}$$

The system ESR zero is:

$$\omega_{ZESR} = \frac{1}{R_C \times C_O} \tag{43}$$

The low frequency pole is:

$$\omega_{LEP} = \frac{1}{0.5 \times (R_O + ESR) \times C_O} \tag{44}$$

The right-half plane zero is:

$$\omega_{RHP} = \frac{R_O \times \left(\frac{V_{IN}}{V_O}\right)^2}{L} \tag{45}$$

The sampling double pole quality factor is:

$$Q_n = \frac{1}{\pi \left[-D + 0.5 + (1 - D)\frac{S_e}{S_n}\right]} \tag{46}$$

The sampling double corner frequency is:

$$\omega_n = \pi \times f_{SW} \tag{47}$$

The natural inductor current slope is:

$$S_n = R_{SNS} \times V_{IN} / L \tag{48}$$

The external ramp slope is:

$$S_e = 45\ \mu A \times (2000 + R_{S1} + R_{S2})] \times f_{SW} \tag{49}$$

In the equation for A_{PS}, DC gain is highest when input voltage is at the maximum and output current is at the lower threshold of CCM operation. ($I_L = 0.5 \times \Delta i_L$) In this the example those conditions are V_{IN} = 20.9V and I_O = 180 mA.

Maximum DC gain is 44 dB. The low frequency pole $f_P = 2\pi\omega_P$ is at 1.9 kHz, the ESR zero $f_Z = 2\pi\omega_Z$ is at 80 MHz, and the right-half plane zero $f_{RHP} = 2\pi\omega_{RHP}$ is at 230 kHz. The sampling double-pole occurs at one-half of the switching frequency. Gain and phase plots for the power stage are shown in Figure 9.

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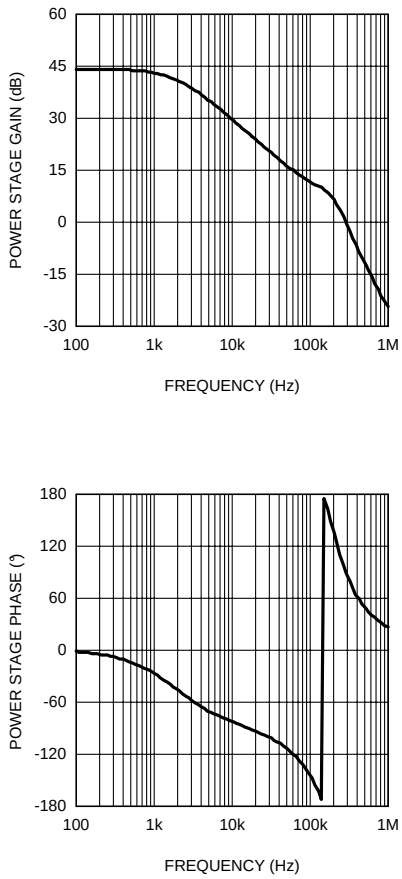

Figure 9. Power Stage Gain and Phase

The single pole causes a roll-off in the gain of -20 dB/decade at lower frequency, which then flattens out due to the RHP zero. The sharp drop in gain beginning around 200 kHz is a result of the sampling double pole. The phase tends towards -90° at lower frequency but then increases to -180° from the RHP zero and the sampling double pole. The effect of the ESR zero is not seen because its frequency is several decades above the switching frequency. The combination of increasing gain and decreasing phase makes converters with RHP zeroes difficult to compensate. Setting the overall control loop bandwidth to 1/3 to 1/10 of the RHP zero frequency minimizes these negative effects. If this loop were left uncompensated, the bandwidth would be 312 kHz and the phase margin -100°. The converter would oscillate, and therefore is compensated using the error amplifier and a few passive components.

The transfer function of the compensation block, G_{EA}, can be derived by treating the error amplifier as an inverting op-amp with input impedance Z_I and feedback impedance Z_F. The majority of applications will require a Type II, or two-pole one-zero amplifier, shown in Figure 8. The LaPlace domain transfer function for this Type II network is given by the following:

$$G_{EA} = \frac{Z_F}{Z_I} = \frac{1}{R_{FB2}\,(C1 + C2)} \times \frac{s \times R1 \times C1 + 1}{s\left(\frac{s \times R1 \times C1 \times C2}{C1 + C2} + 1\right)} \tag{50}$$

Many techniques exist for selecting the compensation component values. The following method is based upon setting the mid-band gain of the error amplifier transfer function first and then positioning the compensation zero and pole:

1. **Determine the desired control loop bandwidth:** The control loop bandwidth, f_{0dB}, is the point at which the total control loop gain ($H = G_{PS} \times G_{EA}$) is equal to 0 dB. For this example, a low bandwidth of 30 kHz, or approximately 1/8th of the RHP zero frequency, is chosen because of the wide variation in input voltage.
2. **Determine the gain of the power stage at f_{0dB}:** This value, A, can be read graphically from the gain plot of G_{PS} or calculated by replacing the 's' terms in G_{PS} with '$2\pi f_{0dB}$'. For this example the gain at 30 kHz is

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approximately 20 dB.

3. **Calculate the negative of A and convert it to a linear gain:** By setting the mid-band gain of the error amplifier to the negative of the power stage gain at f_{0dB}, the control loop gain will equal 0 dB at that frequency. For this example, -20 dB = 0.1V/V.
4. **Select the resistance of the top feedback divider resistor R_{FB2}:** This value is arbitrary, however selecting a resistance between 10 kΩ and 100 kΩ will lead to practical values of R1, C1 and C2. For this example, R_{FB2} = 20 kΩ 1%.
5. **Set R1 = A x R_{FB2}:** For this example: R1 = 0.1 x 20000 = 2 kΩ
6. **Select a frequency for the compensation zero, f_{Z1}:** The suggested placement for this zero is at the low frequency pole of the power stage, $f_{LFP} = \omega_{LFP} / 2\pi$. For this example, $f_{Z1} = f_{LFP}$ = 1.9 kHz
7. **Set** $C2 = \frac{1}{2\pi \times R1 \times f_{Z1}}$: For this example, C2 = 41.2 nF
8. **Select a frequency for the compensation pole, f_P1:** The suggested placement for this pole is at one-half of the switching frequency. For this example, f_{P1} = 200 kHz
9. **Set**

   $$C1 = \frac{C2}{2\pi \times C2 \times R1 \times f_{P1} - 1}:$$

   For this example, C1 = 401 pF
10. **Plug the closest 1% tolerance values for RFB2 and R1, then the closest 10% values for C1 and C2 into G_{EA} and model the error amp:** The open-loop gain and bandwidth of the LM3430's internal error amplifier are 75 dB and 4 MHz, respectively. Their effect on G_{EA} can be modeled using the following expression:

    $$OPG = \frac{2\pi \times GBW}{s + \frac{2\pi \times GBW}{A_{DC}}}$$

    A_{DC} is a linear gain, the linear equivalent of 75 dB is approximately 5600V/V. C1 = 390 pF 10%, C2 = 39 nF 10%, R1 = 2 kΩ 1%
11. **Plot or evaluate the actual error amplifier transfer function:** $G_{EA\text{-}ACTUAL} = \frac{G_{EA} \times OPG}{1 + G_{EA} \times OPG}$

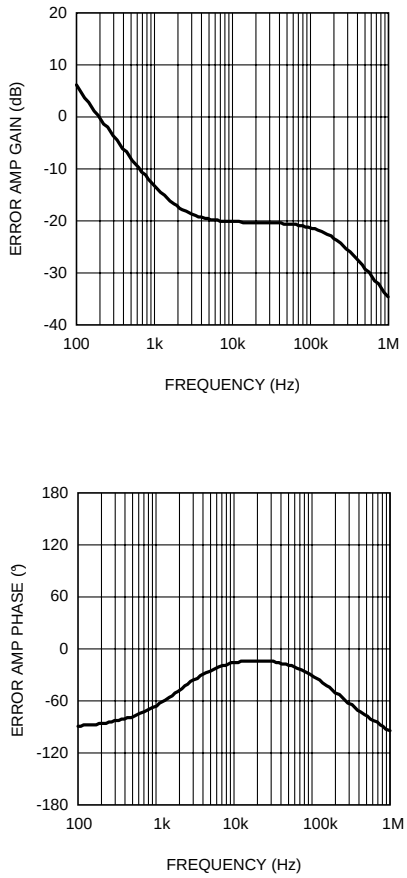

Figure 10. Error Amplifier Gain and Phase

12. Plot or evaluate the complete control loop transfer function: The complete control loop transfer function is obtained by multiplying the power stage and error amplifier functions together. The bandwidth and phase margin can then be read graphically or evaluated numerically.

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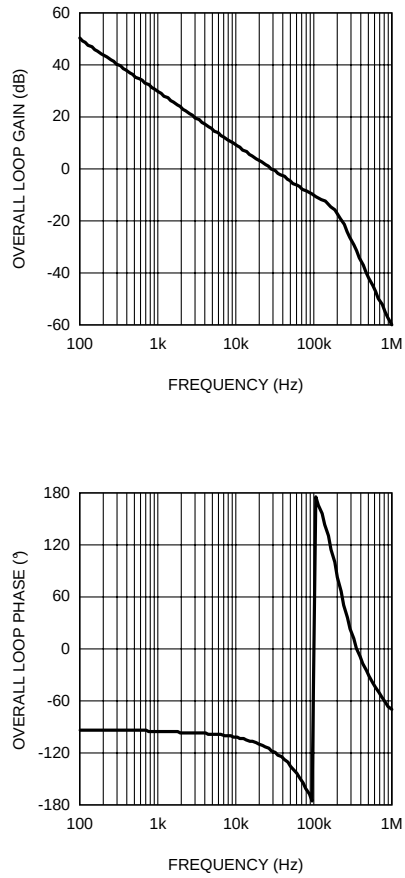

Figure 11. Overall Loop Gain and Phase

The bandwidth of this example circuit is 34 kHz, with a phase margin of 60°.

Efficiency Calculations

A reasonable estimation for the efficiency of a boost regulator controlled by the LM3430 can be obtained by adding together the loss is each current carrying element and using the equation:

$$\eta = \frac{P_O}{P_O + P_{total\text{-}loss}} \tag{51}$$

The following shows an efficiency calculation to complement the circuit design from the Design Considerations section. Output power for this circuit is 33V x 0.18A = 5.9W. Input voltage is assumed to be 12V, and the calculations used assume that the converter runs in CCM. Duty cycle for V_{IN} = 12V is 63%, and the average inductor current is 0.49A.

CHIP OPERATING LOSS

This term accounts for the current drawn at the VIN pin. This current, I_{IN}, drives the logic circuitry and the power MOSFETs. The gate driving loss term from the power MOSFET section of Design Considerations is included in the chip operating loss. For the LM3430, I_{IN} is equal to the steady state operating current, I_{CC}, plus the MOSFET driving current, I_{GC}. Power is lost as this current passes through the internal linear regulator of the LM3430.

$$I_{GC} = Q_G \text{ X } f_{SW} \; I_{GC} = 18 \text{ nC x } 600 \text{ kHz} = 11 \text{ mA} \tag{52}$$

I_{CC} is typically 3.5 mA, taken from the Electrical Characteristics table. Chip Operating Loss is then:

$P_Q = V_{IN} X (I_Q + I_{GC})$ $P_Q = 12 X (3.5m + 11m) = 0.17W$ (53)

MOSFET SWITCHING LOSS

$P_{SW} = 0.5 x V_{IN} x I_L x (t_R + t_F) x f_{SW}$ $P_{SW} = 0.5 x 12 x 0.49 x (10 ns + 12 ns) x 6 x10^5 = 39 mW$ (54)

MOSFET AND R_{SNS} CONDUCTION LOSS

$P_C = D x (I^2_L x (R_{DSON} x 1.3 + R_{SNS}))$ $P_C = 0.63 x (0.49^2 x (0.029 + 0.51) = 82 mW$ (55)

INPUT CAPACITOR LOSS

This term represents the loss as input ripple current passes through the ESR of the input capacitor bank. In this equation 'n' is the number of capacitors in parallel. The 3.3 µF input capacitor selected has an ESR of approximately 3 mΩ, and Δi_L for a 12V input is 268 mA:

$$P_{CIN} = \frac{I^2_{IN\text{-}RMS} x ESR}{n} \quad (56)$$

$I_{IN\text{-}RMS} = 0.29 x \Delta i_L = 0.29 x 0.268 = 0.08A$ $P_{CIN} = 0.08^2 x 0.003 = 0.3 mW$ (negligible) (57)

OUTPUT CAPACITOR LOSS

This term is calculated using the same method as the input capacitor loss, substituting the output capacitor RMS current for V_{IN} = 12V:

$I_{O\text{-}RMS} = 1.13 x 0.49 x (0.37 x 0.63)^{0.5} = 0.267A$ $P_{CO} = 0.267 x 0.003 = 1 mW$ (58)

BOOST INDUCTOR LOSS

$P_{DCR} = I_L^2 x DCR$ $P_{DCR} = 0.49^2 x 0.18 = 43 mW$ (59)

Core loss in the inductor is assumed to be equal to the DCR loss, adding an additional 43 mW to the total inductor loss.

TOTAL LOSS

P_{LOSS} = Sum of All Loss Terms = 0.38W (60)

EFFICIENCY

$\eta = 5.9/(5.9 + 0.38) = 94\%$ (61)

Layout Considerations

To produce an optimal power solution with the LM3430, good layout and design of the PCB are as important as the component selection. The following are several guidelines to aid in creating a good layout.

FILTER CAPACITORS

The low-value ceramic filter capacitors are most effective when the inductance of the current loops that they filter is minimized. Place C_{INX} as close as possible to the VIN and GND pins of the LM3430. Place C_{OX} close to the load. C_{CS} should be placed right next to R_{SNS}, and C_F next to the VCC and GND pins of the LM3430.

SENSE LINES

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The top of R_{SNS} should be connected to the CS pin with a separate trace made as short as possible. Route this trace away from the inductor and the switch node (where D1, Q1, and L1 connect). For the voltage loop, keep $R_{FB1/2}$ close to the LM3430 and run a trace from as close as possible to the positive side of C_{OX} to R_{FB2}. As with the CS line, the FB line should be routed away from the inductor and the switch node. These measures minimize the length of high impedance lines and reduce noise pickup.

COMPACT LAYOUT

Parasitic inductance can be reduced by keeping the power path components close together and keeping the area of the loops that high currents travel small. Short, thick traces or copper pours (shapes) are best. In particular, the switch node should be just large enough to connect all the components together without excessive heating from the current it carries. The LM3430 (boost converter) operates in two distinct cycles whose high current paths are shown in Figure 12:

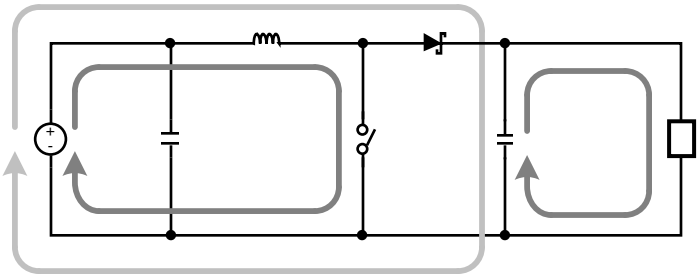

Figure 12. Boost Converter Current Loops

The dark grey, inner loops represents the high current paths during the MOSFET on-time. The light grey, outer loop represents the high current path during the off-time.

GROUND PLANE AND SHAPE ROUTING

The diagram of Figure 12 is also useful for analyzing the flow of continuous current vs. the flow of pulsating currents. The circuit paths with current flow during both the on-time and off-time are considered to be continuous current, while those that carry current during the on-time or off-time only are pulsating currents. Preference in routing should be given to the pulsating current paths, as these are the portions of the circuit most likely to emit EMI. The ground plane of a PCB is a conductor and return path, and it is susceptible to noise injection just as any other circuit path. The continuous current paths on the ground net can be routed on the system ground plane with less risk of injecting noise into other circuits. The path between the input source, input capacitor and the power switch and the path between the output capacitor and the load are examples of continuous current paths. In contrast, the path between the grounded side of the power switch and the negative output capacitor terminal carries a large pulsating current. This path should be routed with a short, thick shape, preferably on the component side of the PCB. Multiple vias in parallel should be used right at the negative pads of the input and output capacitors to connect the component side shapes to the ground plane. Vias should not be placed directly at the grounded side of the power switch (or R_{SNS}) as they tend to inject noise into the ground plane.A second pulsating current loop that is often ignored but must be kept small is the gate drive loop formed by the OUT and VCC pins, Q1, R_{SNS} and capacitor C_F.

BOM for Example Circuit

ID	Part Number	Type	Size	Parameters	Qty	Vendor
U1	LM3430	Low-Side Controller	LLP-12		1	NSC
Q1	Si4850EY	MOSFET	SO-8	60V, 31mΩ, 18nC	1	Vishay
D1	CMHSH5-4	Schottky Diode	SOD-123	40V, 0.5A	1	Central Semi
L1	SLF7045T-470M90-1PF	Inductor	7.0 x7.0 x 4.5mm	47µH, 0.9A, 180mΩ	1	TDK
Cin	C3216X7R1E335M	Capacitor	1206	3.3µF, 25V, 3mΩ	1	TDK
Co	C3216X7R1H105M	Capacitor	1206	1µF, 50V, 3mΩ	1	TDK

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ID	Part Number	Type	Size	Parameters	Qty	Vendor
Cf	C2012X7R1E105K	Capacitor	0805	1µF, 25V	1	TDK
Cinx Cox	VJ0805Y104KXXAT	Capacitor	0805	100nF 10%	1	Vishay
C1	VJ0805A391KXXAT	Capacitor	0805	390pF 10%	1	Vishay
C2	VJ0805Y393KXXAT	Capacitor	0805	39nF 10%	1	Vishay
Css	VJ0805Y103KXXAT	Capacitor	0805	10nF 10%	1	Vishay
Ccs	VJ0805Y102KXXAT	Capacitor	0805	1nF 10%	1	Vishay
R1	CRCW08052001F	Resistor	0805	2kΩ 1%	1	Vishay
Rfb1	CRCW08057870F	Resistor	0805	787Ω 1%	1	Vishay
Rfb2	CRCW08052002F	Resistor	0805	20kΩ 1%	1	Vishay
Rs1	CRCW0805101J	Resistor	0805	100Ω 5%	1	Vishay
Rsns	ERJ8BQFR51V	Resistor	1206	0.51Ω 1%, 0.33W	1	Panasonic
Rt	CRCW08052742F	Resistor	0805	27.4kΩ 1%	1	Vishay
Ruv1 Ruv2	CRCW08051002F	Resistor	0805	10kΩ 1%	2	Vishay

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM3430SD	ACTIVE	WSON	DQB	12	1000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 125	L3430	Samples
LM3430SD/NOPB	ACTIVE	WSON	DQB	12	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L3430	Samples
LM3430SDX	ACTIVE	WSON	DQB	12	4500	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 125	L3430	Samples
LM3430SDX/NOPB	ACTIVE	WSON	DQB	12	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L3430	Samples

(1) The marketing status values are defined as follows:
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LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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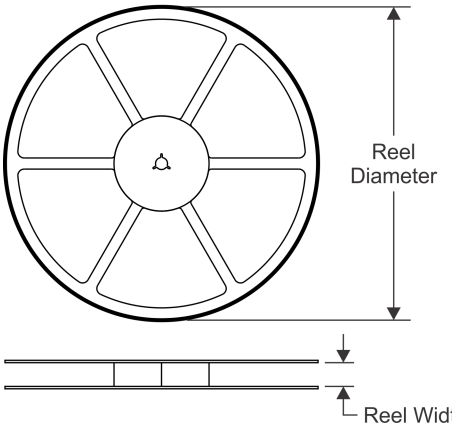

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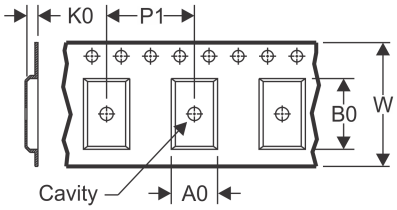
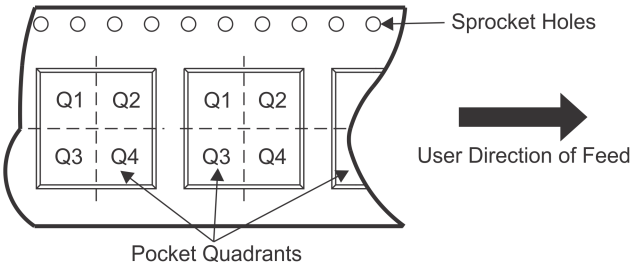


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

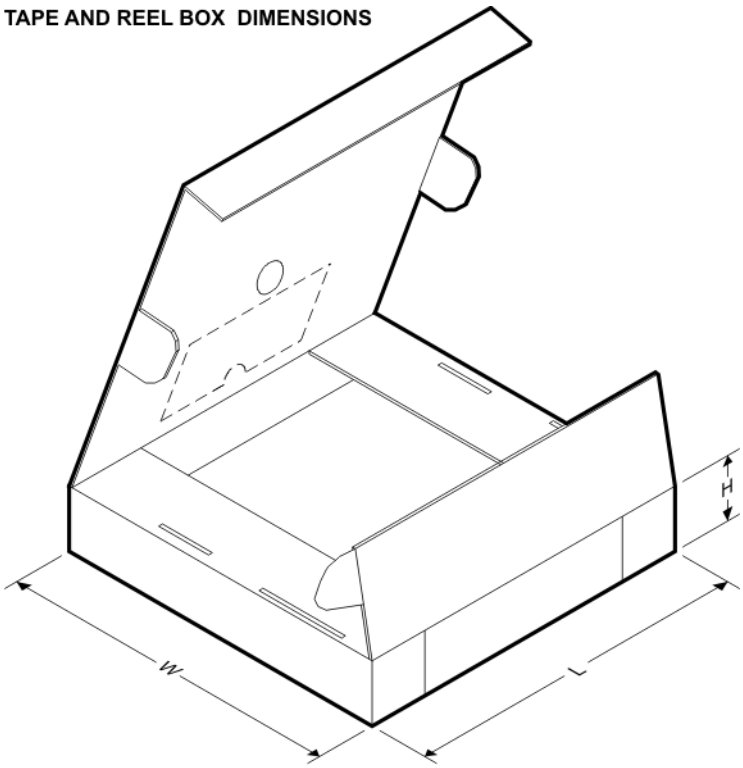
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3430SD	WSON	DQB	12	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM3430SD/NOPB	WSON	DQB	12	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM3430SDX	WSON	DQB	12	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM3430SDX/NOPB	WSON	DQB	12	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

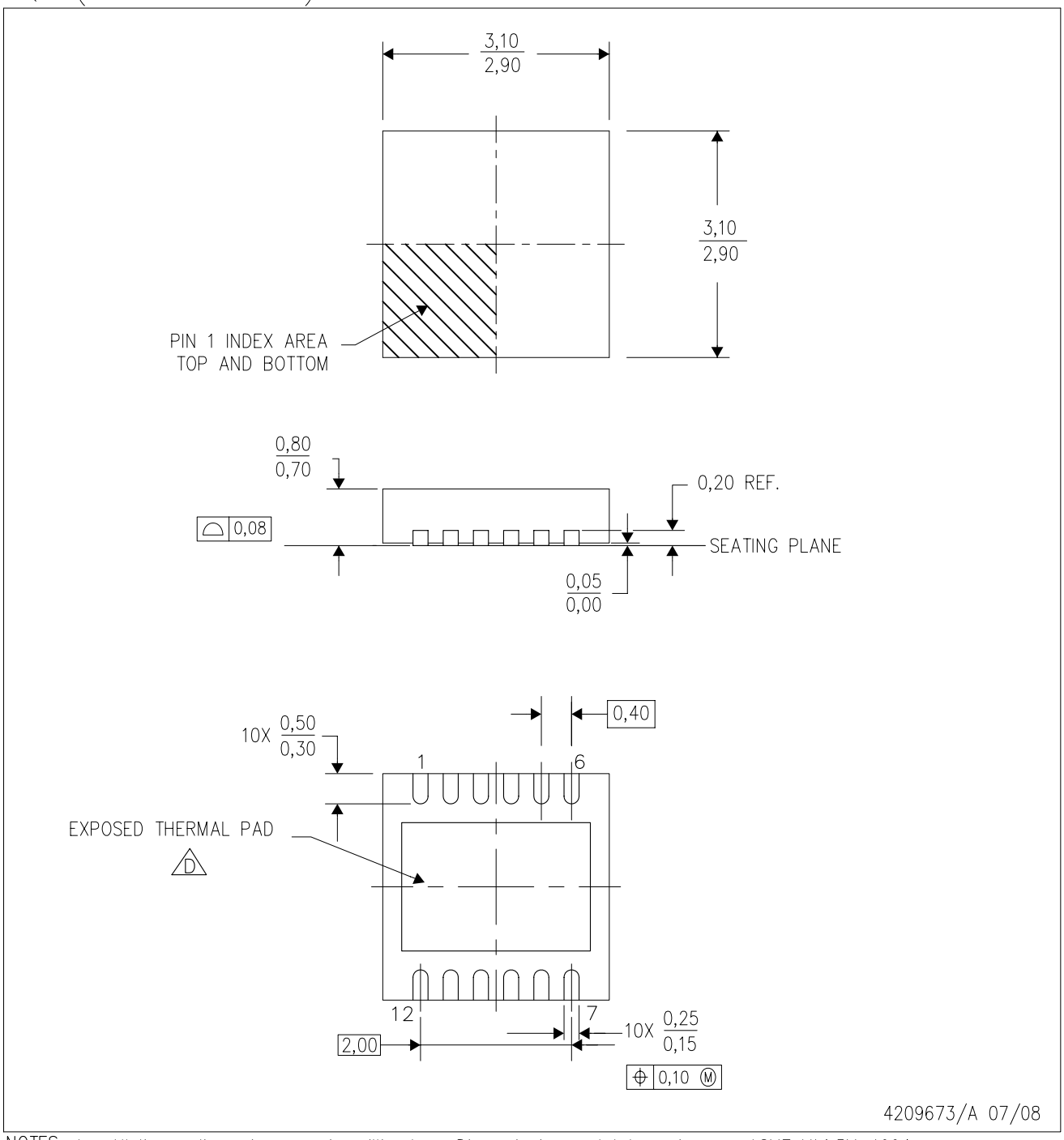
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3430SD	WSON	DQB	12	1000	203.0	190.0	41.0
LM3430SD/NOPB	WSON	DQB	12	1000	203.0	190.0	41.0
LM3430SDX	WSON	DQB	12	4500	349.0	337.0	45.0
LM3430SDX/NOPB	WSON	DQB	12	4500	349.0	337.0	45.0

DQB (S-PWSON-N12) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Small Outline No-Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

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